--~~41~~ 21. The method as claimed in claim ~~34~~ 19, wherein said heat-treating the element insulating layer step is performed at a temperature which discharges fluorine in the element insulating layer without reacting the fluorine and silicon in the semiconductor device.--

Please charge the fee of $18 for the extra claim of any type added herewith, to Deposit Account No. 25-0120.

R E M A R K S

The specification and abstract have been amended as to form to place the application in condition for allowance at the time of the next Official Action.

Figures 3(a), 3(b), 3(c), 3(d), 3(e), 3(f), 3(g), 4, 5(a), and 5(b) of the drawings are proposed to be amended by the accompanying REQUEST FOR PERMISSION TO MAKE DRAWING CORRECTIONS letter which identifies these figures as prior art. Formal drawings will be submitted after receipt of the Notice of Allowance.

The Official Action rejected claims 1-10 and 15-16 under §103(a) as unpatentable over CHIANG et al. 5,707,896 in view of WOLF ("Silicon Processing for the VLSI Era", Vol. 2, 1990, pages 144-147); and rejected claims 11-14 and 17-20 under §103(a)as unpatentable over CHIANG et al. and WOLF in further view of KITANO 5,665,646.

Claims 1-20 have been replaced by claims 21-41 to clarify the steps of applicant's invention.

--41. The method as claimed in claim 34, wherein said heat-treating the element insulating layer step is performed at a temperature which discharges fluorine in the element insulating layer without reacting the fluorine and silicon in the semiconductor device.--

Please charge the fee of $18 for the extra claim of any type added herewith, to Deposit Account No. 25-0120.

R E M A R K S

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Claims 1-20 have been replaced by claims 21-41 to clarify the steps of applicant's invention.

Independent claim 21 recites heat-treating the element insulating layer to decrease a fluorine concentration in the element insulating layer to a level less than 1 x 10^{20} atoms/cm^2, forming a metal layer on the gate electrode, and heat-treating the metal layer and the gate electrode to form a metal silicide on the gate electrode, wherein heat-treatment of the element insulating layer is performed before forming the metal layer. These features are disclosed at page 10, line 26 through page 12, line 16, and are not taught or suggested by the applied art.

Similarly, independent claim 27 recites heat-treating the element insulation layer at a temperature which discharges fluorine in the element isolation layer without reacting the fluorine and silicon in the element isolation layer, forming a metal layer on the gate electrode, and heat-treating the metal layer and the gate electrode to form a metal silicide on the gate electrode, wherein heat-treating of the element isolation layer step is performed before forming the metal layer. Likewise, the applied art does not teach or suggest these steps.

Independent claim 34 recites forming a surface insulating layer over an entire surface of the substrate, injecting an ion injection species into the substrate using the gate electrode as a mask, heat-treating the element insulation layer at a temperature which decreases a fluorine concentration in the element isolation layer, removing the surface insulating layer, forming a metal layer on the gate

electrode, and heat-treating the metal layer and the gate electrode to form a metal silicide on the gate electrode.

The applied art does not teach or suggest all of these steps.

For example, CHIANG et al. do not disclose heat-treating the element insulating layer before forming a metal layer to decrease a fluorine concentration in the element insulating layer (to a level less than 1 x 10^{20} atoms/cm^2 as in claim 21), nor do they disclose heat-treating the metal layer and the gate electrode to form a metal silicide on the gate electrode (at a temperature higher than the heat-treatment of the element insulating layer as in dependent claim 25).

WOLF is offered as disclosing deposition and reaction of a metal layer to form a silicide, which is acknowledged as being known in the art, however WOLF, neither alone, or in combination, teaches or suggests a novel feature of applicant's invention as recited in independent claims 21, 37, and 34, i.e. heat-treating the element insulating layer before forming a metal layer to decrease a fluorine concentration in the element insulating layer. Further, applicant respectfully suggests that motivation to combine the teachings of CHIANG et al. with WOLF is lacking for the reasons below.

CHIANG et al. merely describe annealing polysilicon gate electrodes 20 before forming interlevel insulating layers of silicon nitride 36 and BPSG 38 (see column 5, line 48 through column 6, line 15, and Figs. 2-4). CHIANG et al.

teach a solution to a different technical problem than applicant's invention, i.e. delamination between a doped poly-silicon film and an overlying interlevel dielectric layer (see Abstract and column 3, lines 49-56), and not a "rising up" of silicide. Therefore, there would be no motivation to modify the method of CHIANG et al. to that of the invention.

Applicant's invention, as recited in claims 21, 27, and 34, is directed to eliminating short circuits between the gate electrode and diffusion layers, and between diffusion layers due to the "rising up" reaction of a silicide formed during metallization (see page 3, lines 10-22; and page 7, lines 3-13). Thus, applicant's method uses steps directed to achieve these different technical objectives.

Therefore, there appears to be no relevance between the processes disclosed in CHIANG et al. and applicant's method as shown in Figures 1(a)-1(h), beyond the fact that both approaches outgas fluorine as only one step, albeit for different reasons, and with different subsequent steps as recited in applicant's claims 21, 27, and 34.

As discussed above, WOLF is offered as disclosing forming a metal silicide layer on the gate electrode and diffusion areas. However, the short circuit problem resulting from fluorine remaining after ion implantation, the factor responsible for the silicide "rising-up" phenomenon (see page 6, lines 15-21), is not recognized by WOLF (nor is a solution to this problem taught or suggested).

Due to the differences between the invention and the applied art as discussed above, applicant respectfully suggests that a person of ordinary skill in the art would lack motivation to modify CHIANG et al., and combine it with WOLF and KITANO.

Therefore, since the applied art does not teach or suggest all the steps and features of applicant's invention as recited in claims 21, 27, and 34, consideration and allowance of these claims are respectfully solicited.

New claims 22-26, 28-33, and 35-41, depending from claims 21, 27, and 34, respectively, recite additional features of applicant's invention, as disclosed in the original written description.

For example, claims 23, 29, and 36 recite injecting ions of BF_2 (see page 11, line 10+); claims 24, 30, and 37 recite heat-treating the element insulator/isolation layer at a temperature of 700°C (see page 11, line 21+); and claims 25, 32, and 39 recite heat-treating to activate the ion injection species at a temperature higher than the step which heat-treats the element insulator/isolation layer to decrease the fluorine concentration in the device (see page 12, line 6+).

These features, when considered in conjunction with the respective independent claims, are not taught or suggested by the applied art. Therefore, consideration and allowance of claims 22-26, 28-33, and 35-41 are respectfully requested.

In light of the above remarks and the accompanying amendment, applicant believes that the present application is

in condition for allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires clarification, the Examiner may contact the undersigned attorney so that this application may continue to be expeditiously advanced.

Respectfully submitted,

YOUNG & THOMPSON

By _____

Roland E. Long, Jr.
Attorney for Applicant
Registration No. 41,949
745 South 23rd Street
Arlington, VA 22202
Telephone: 703/521-2297

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